Formal Abstractions for Attested Execution Secure Processors

Eurocrypt

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Trusted hardware:

Different communities, different world views

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Crypto

Architecture + Systems & Security

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- "Minimal" trusted hardware to circumvent theoretical impossibilities
- Little concern about practical performance

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- "Minimal" trusted hardware to circumvent theoretical impossibilities
- Little concern about practical performance

Architecture + Systems & Security

- Trusted execution of "general-purpose" user-defined progs
- Cost-effectiveness, reusability, expressivity

Architecture community converged on “attested execution”

Bastion

GhostRider

Iso-X

Ascend

Sanctum

Aegis

XOM

Phantom

Academia

TPM

Intel® SGX

TrustZone®
Security Foundation by ARM®

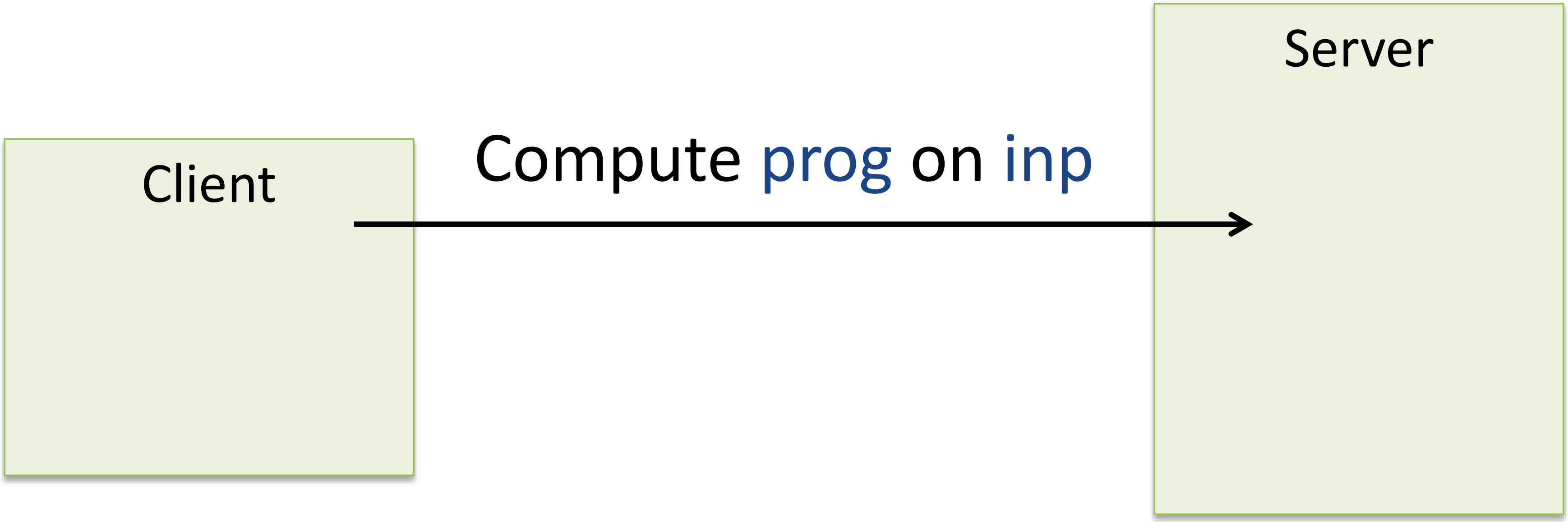
Industry

Architecture community converged on "attested execution"

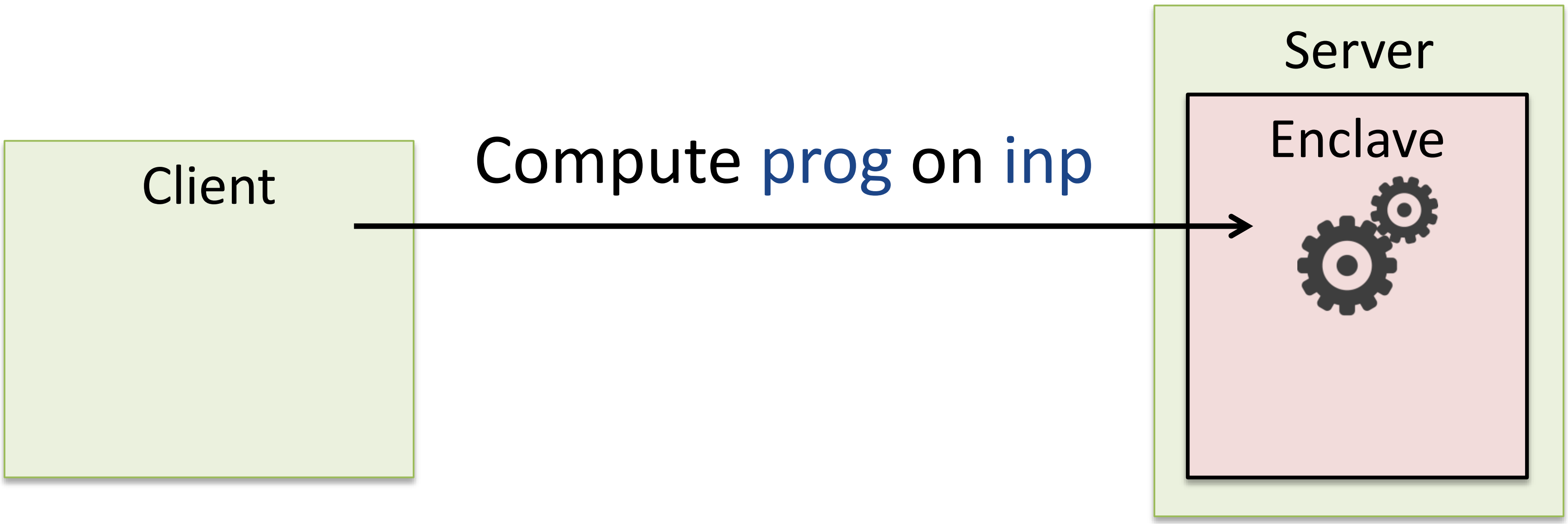
What is "attested execution" ?

What can it (not) express?

Attested Execution



Attested Execution



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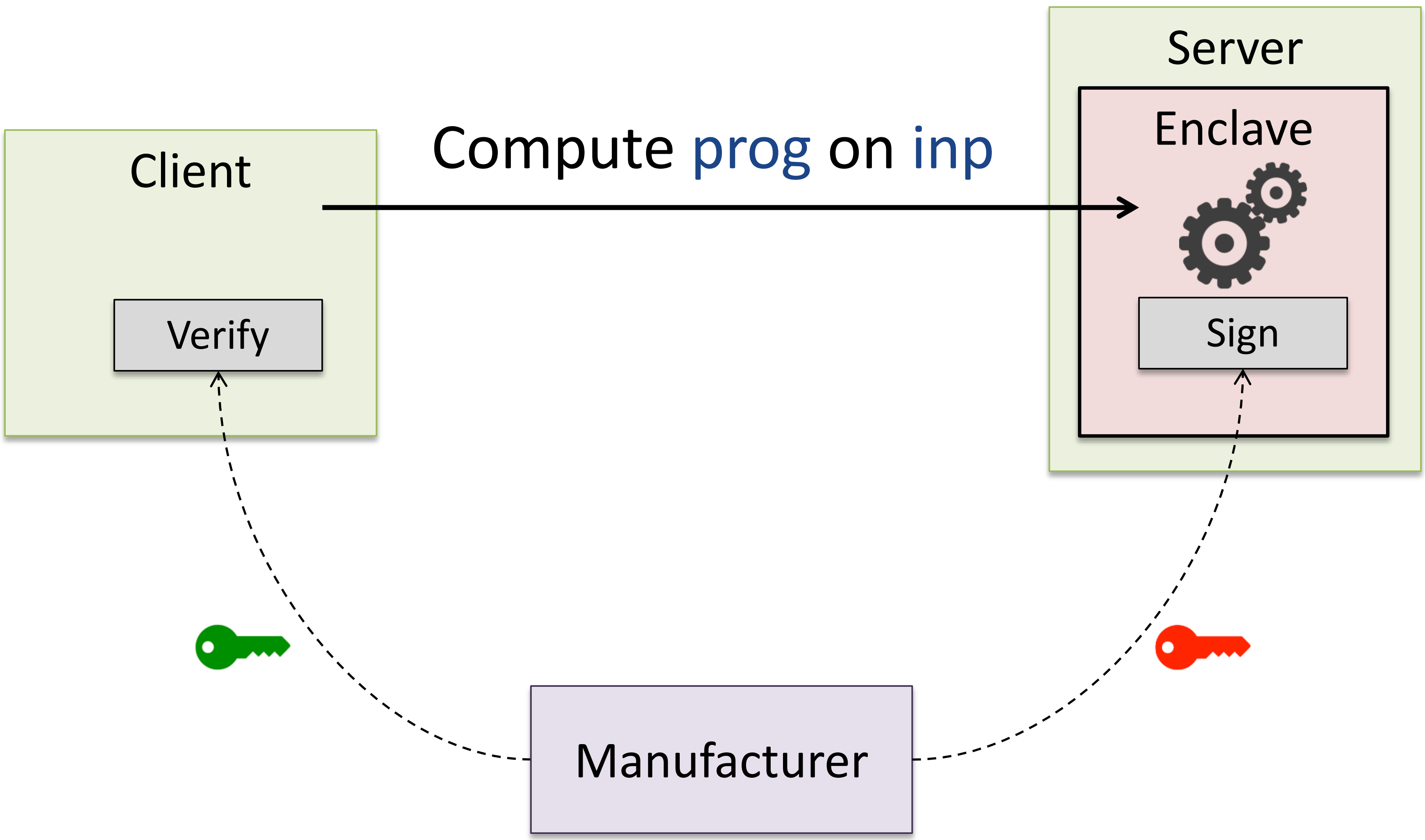

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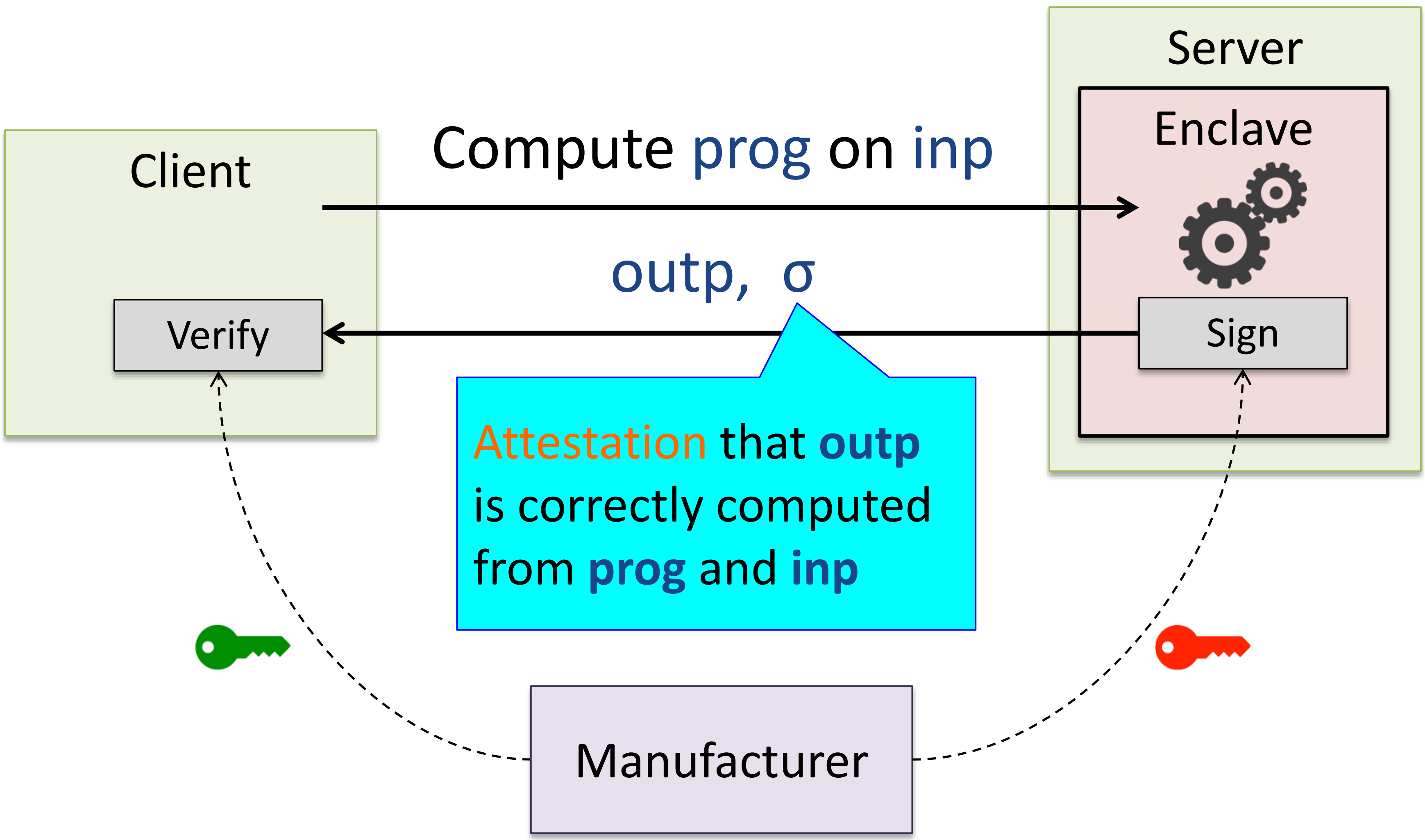

Why Ideal Abstractions?

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- Formal security proofs for implementations from precise abstractions and security models

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- **Ultimate Goal:** Formally verified processor implementing this formal abstraction

Formal Model

Signature scheme

Registry of all platforms with trusted hardware

$$\boldsymbol{\mathcal{G}_{\text{att}}[\Sigma, \text{reg}]}$$

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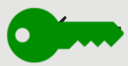
init():   $\leftarrow \Sigma.\mathrm{KeyGen}(1^{\lambda})$

getpk() from P: send  to P

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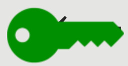
init():   $\leftarrow \Sigma.\mathrm{KeyGen}(1^{\lambda})$

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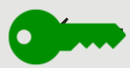
init():   Σ.KeyGen(1^λ)

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enclave memory

(eid, P)	(sid, prog, M)
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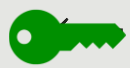
init():   Σ.KeyGen(1^λ)

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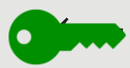
init():   $\Sigma.\mathrm{KeyGen}(1^\lambda)$

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(out, M') = prog(inp, M)

enclave id (nonce) | enclave memory

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(out, M′) = prog(inp, M)

σ = Σ.Sign(, eid, sid, prog, out)

send (out, σ) *to P*

Composability with Global State

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Model $\mathcal{G}_{\text{att}}$ as *global* ideal functionality [CDPW'07]

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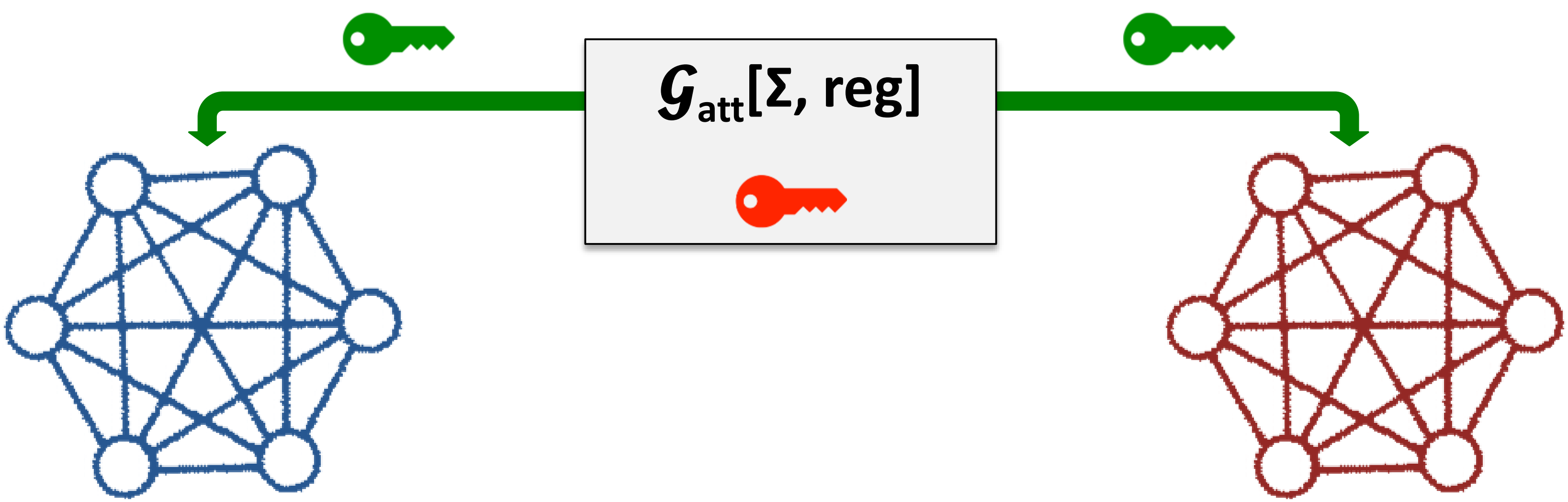
Attestation key is ***shared*** across protocols



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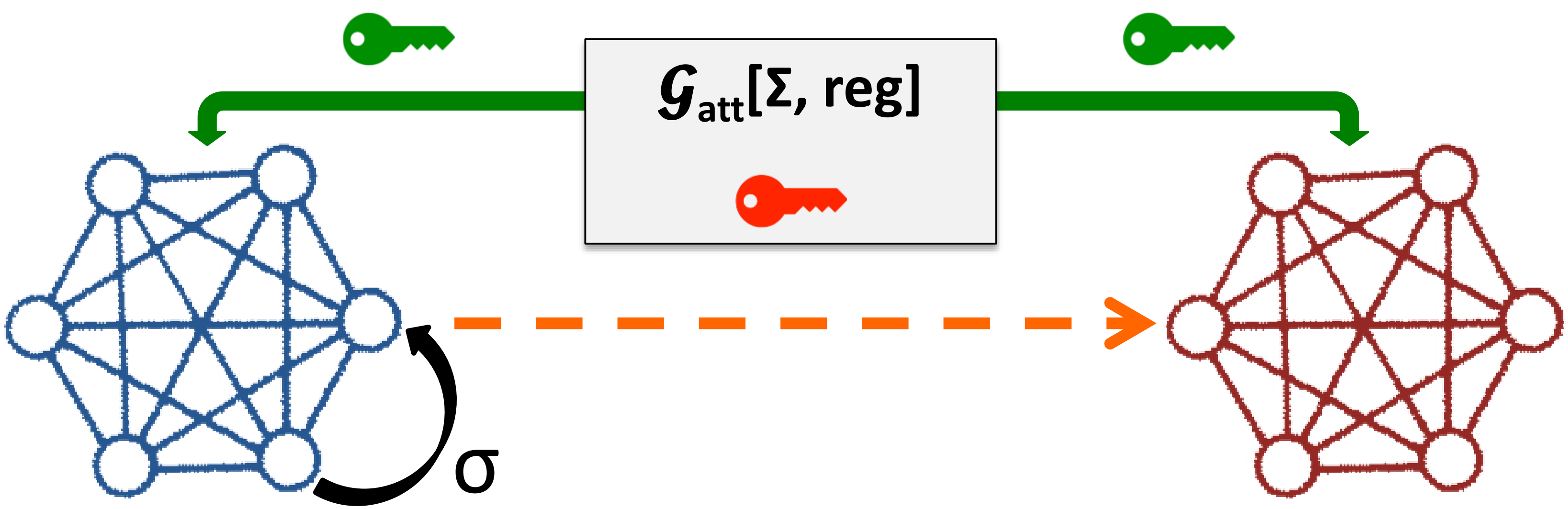
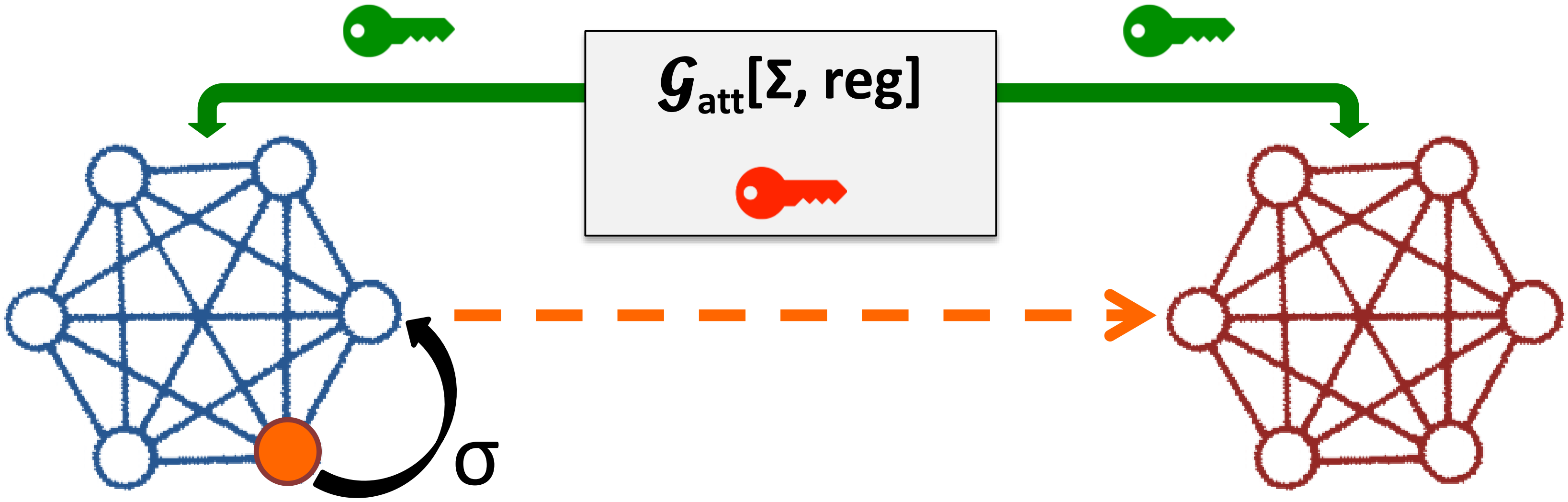


Composability with Global State

Model $\mathcal{G}_{\text{att}}$ as *global* ideal functionality [CDPW'07]

Example of concrete security issue:

Non-deniability for parties in **reg**



The more interesting question

What is “attested execution” ?

What can it **(not)** express?

The good

Powerful Abstraction!

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$\mathcal{G}_{\text{att}} \rightarrow$ "Stateful Obfuscation"

Impossible even with stateless tokens and cryptographic obfuscation

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The surprise

UC-Secure MPC?

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☑ It's Complicated

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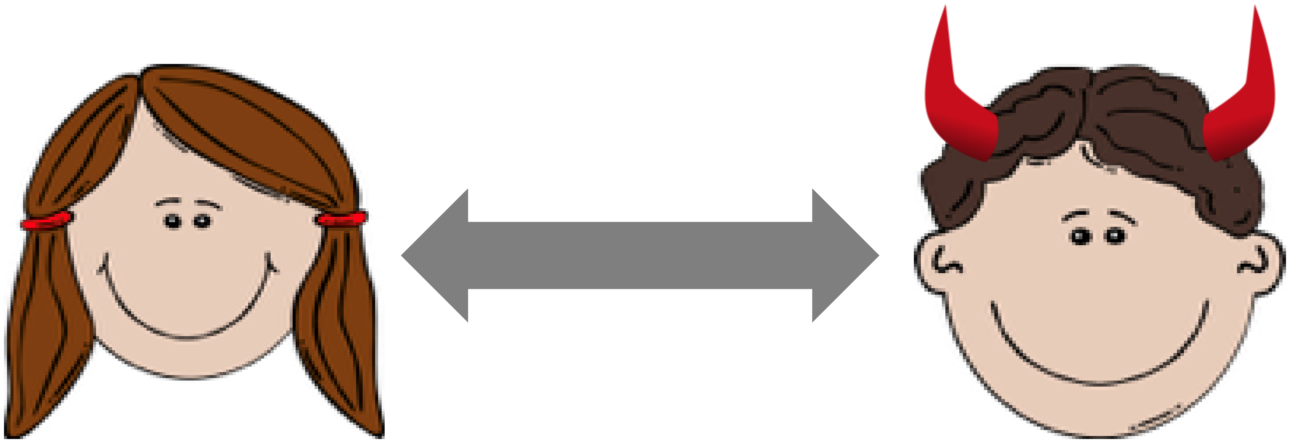
Consider 2PC



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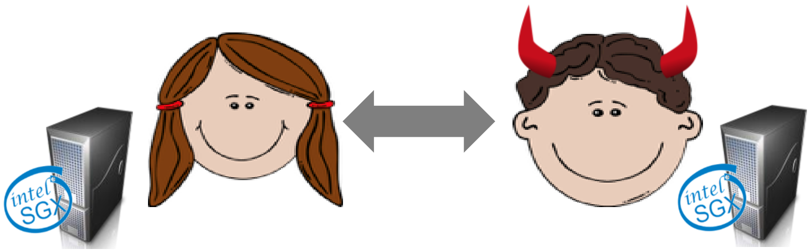

UC-secure 2PC possible if both parties have trusted hardware

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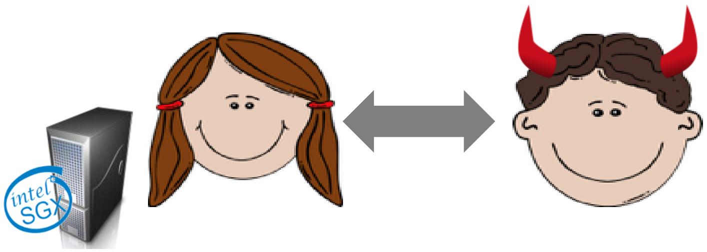

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Impossible if only one party has trusted hardware!

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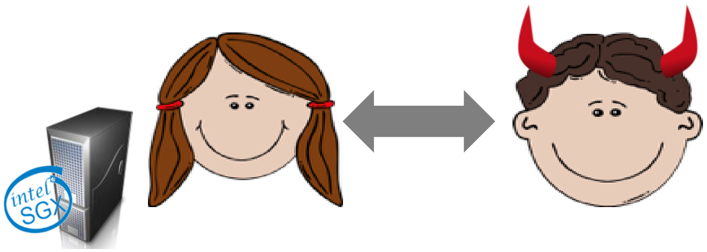

This is counter-intuitive.

Impossible if only one party has trusted hardware!

Issue: non-deniability

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Convinced that
some honest party in the registry
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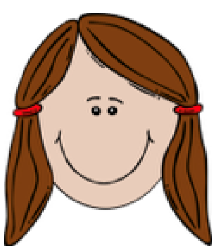

σ under **global pk**

σ

Non-issue if all nodes have trusted hardware
or if pk isn't global

Convinced that
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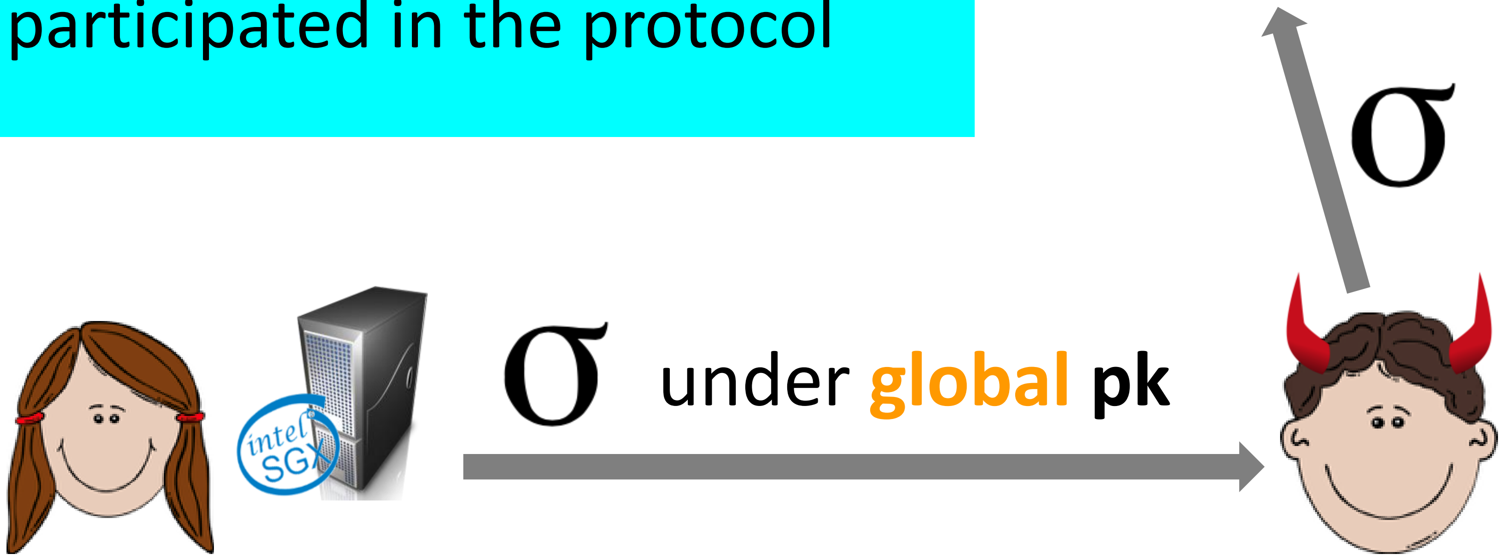

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Extra setup assumption: Augmented CRS

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Backdoor enclave program: allow simulator to *extract inputs* and *program the outputs* for corrupt parties

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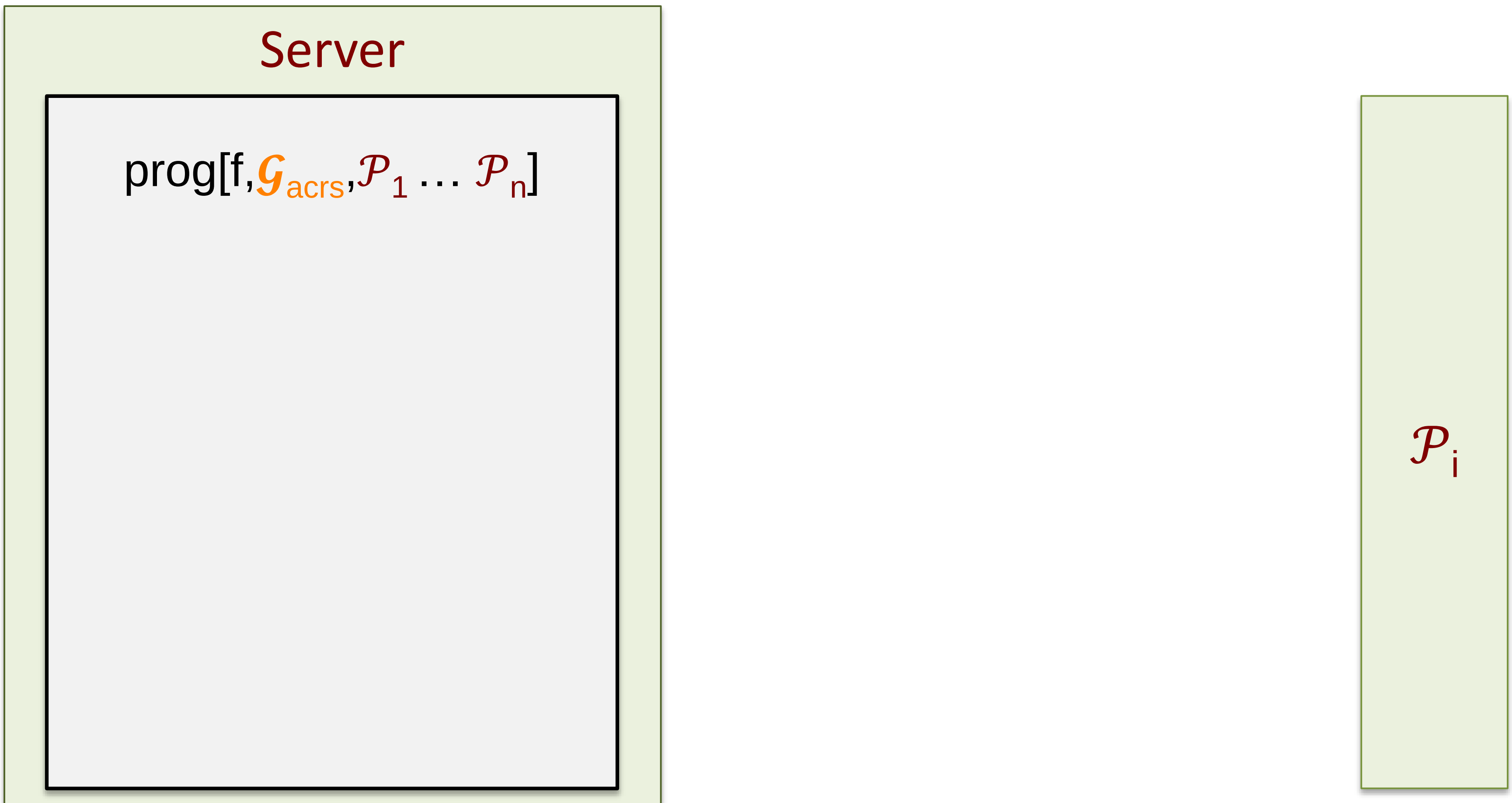

What if we **really really** want to use a single trusted processor?

Server

prog[f,$\mathcal{G}_{acrs}$,$\mathcal{P}_1$ … $\mathcal{P}_n$]

1. Generate pk_i,sk_i

$\mathcal{P}_i$

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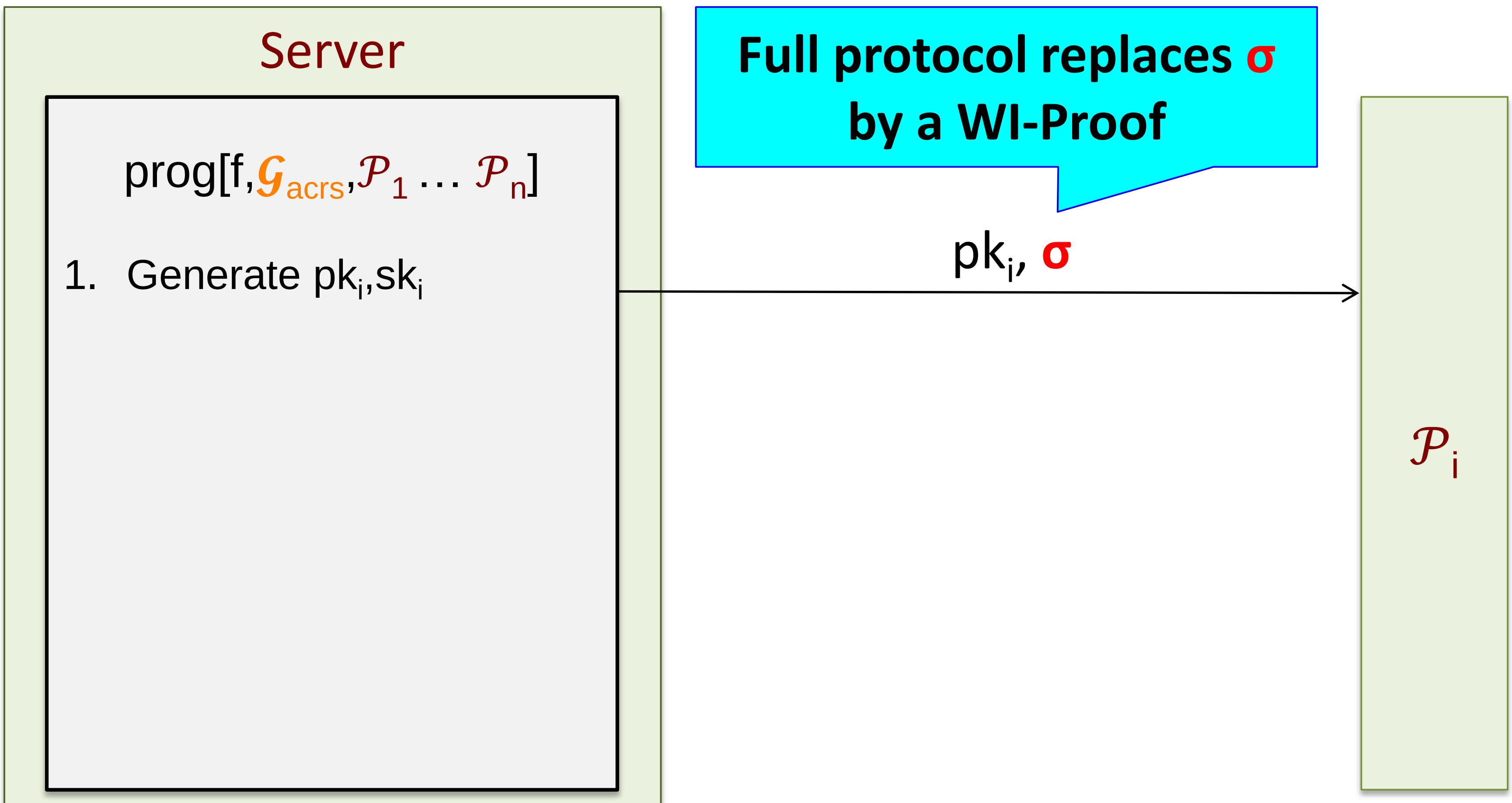

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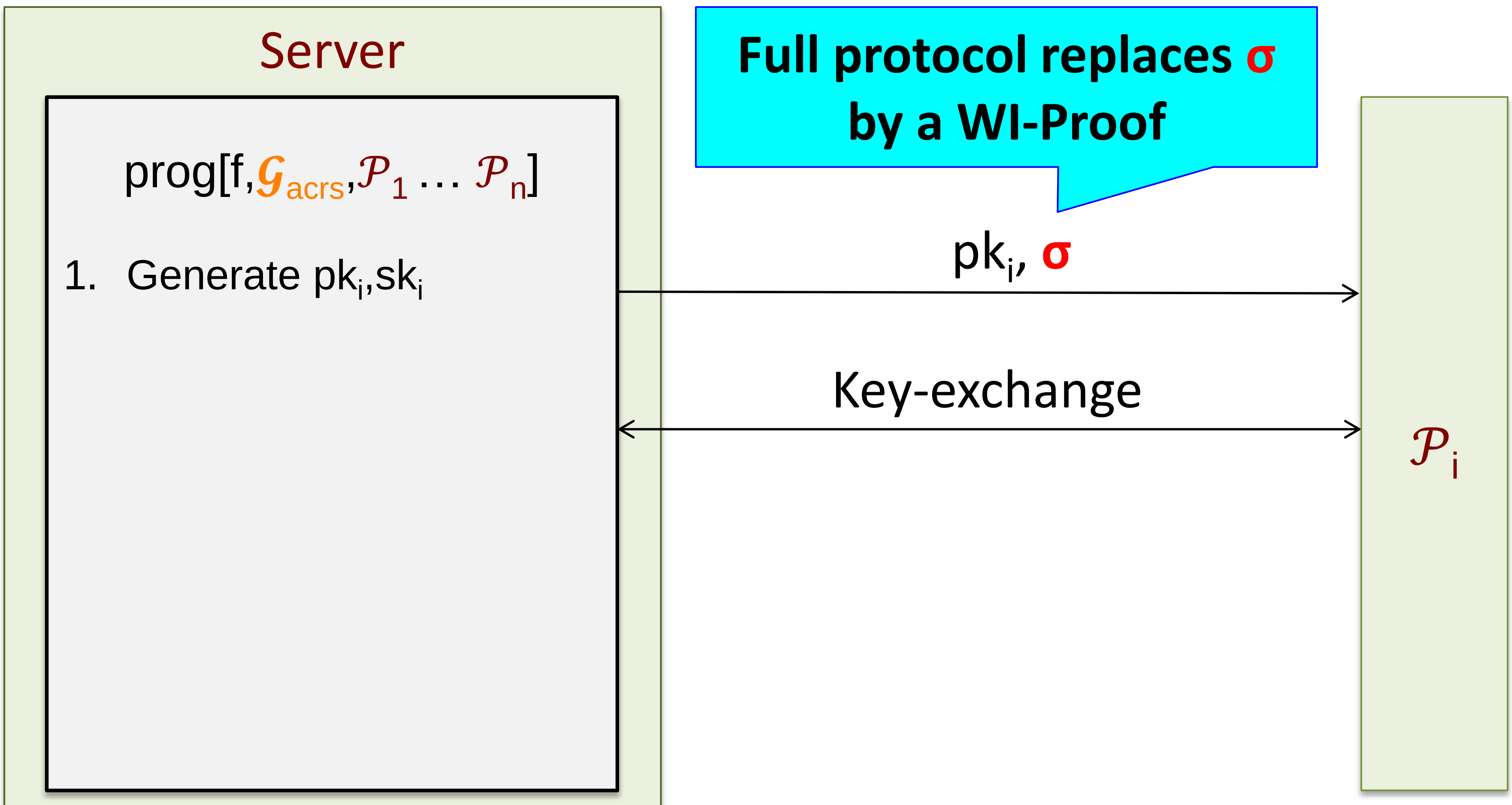

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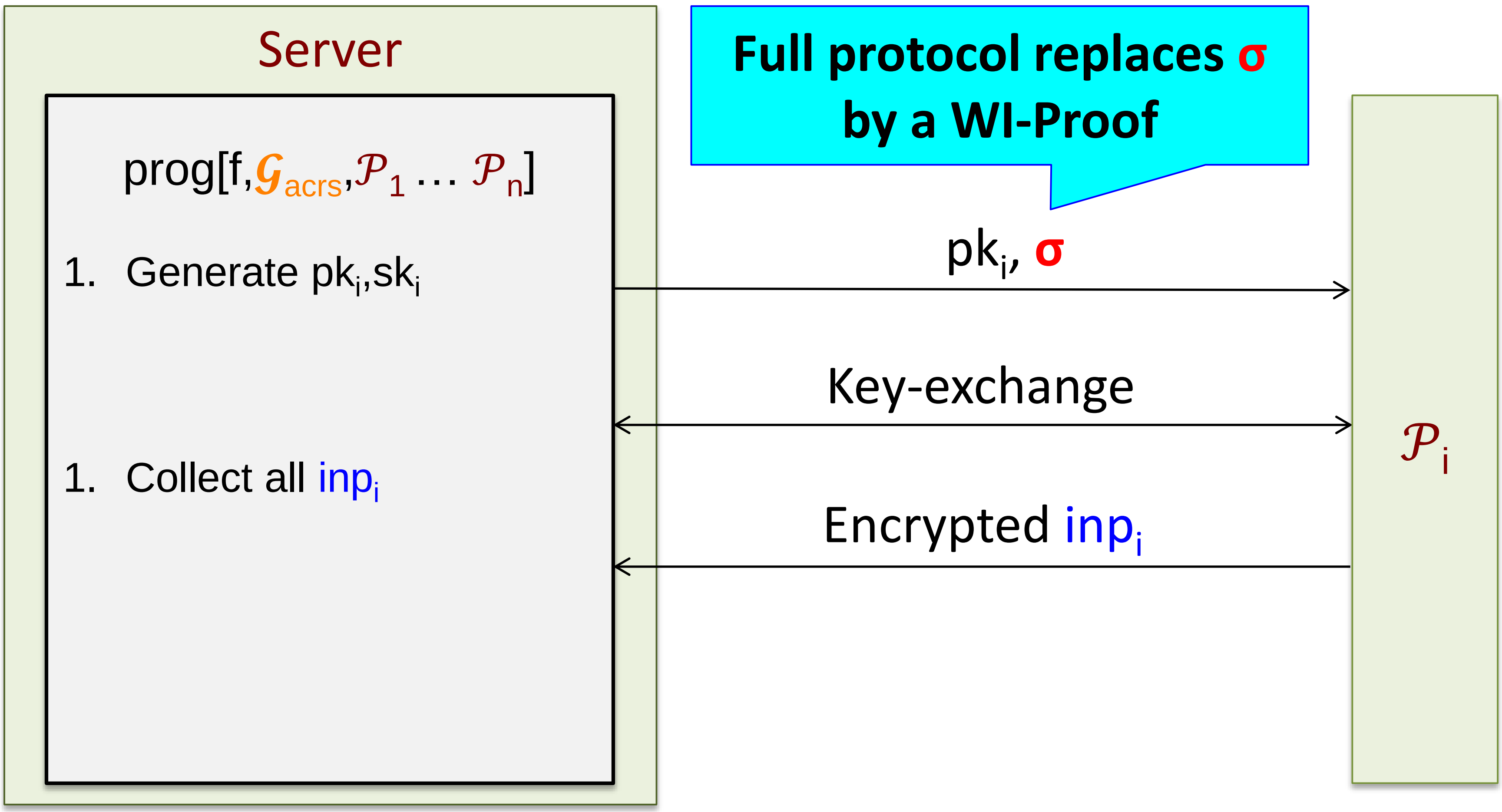

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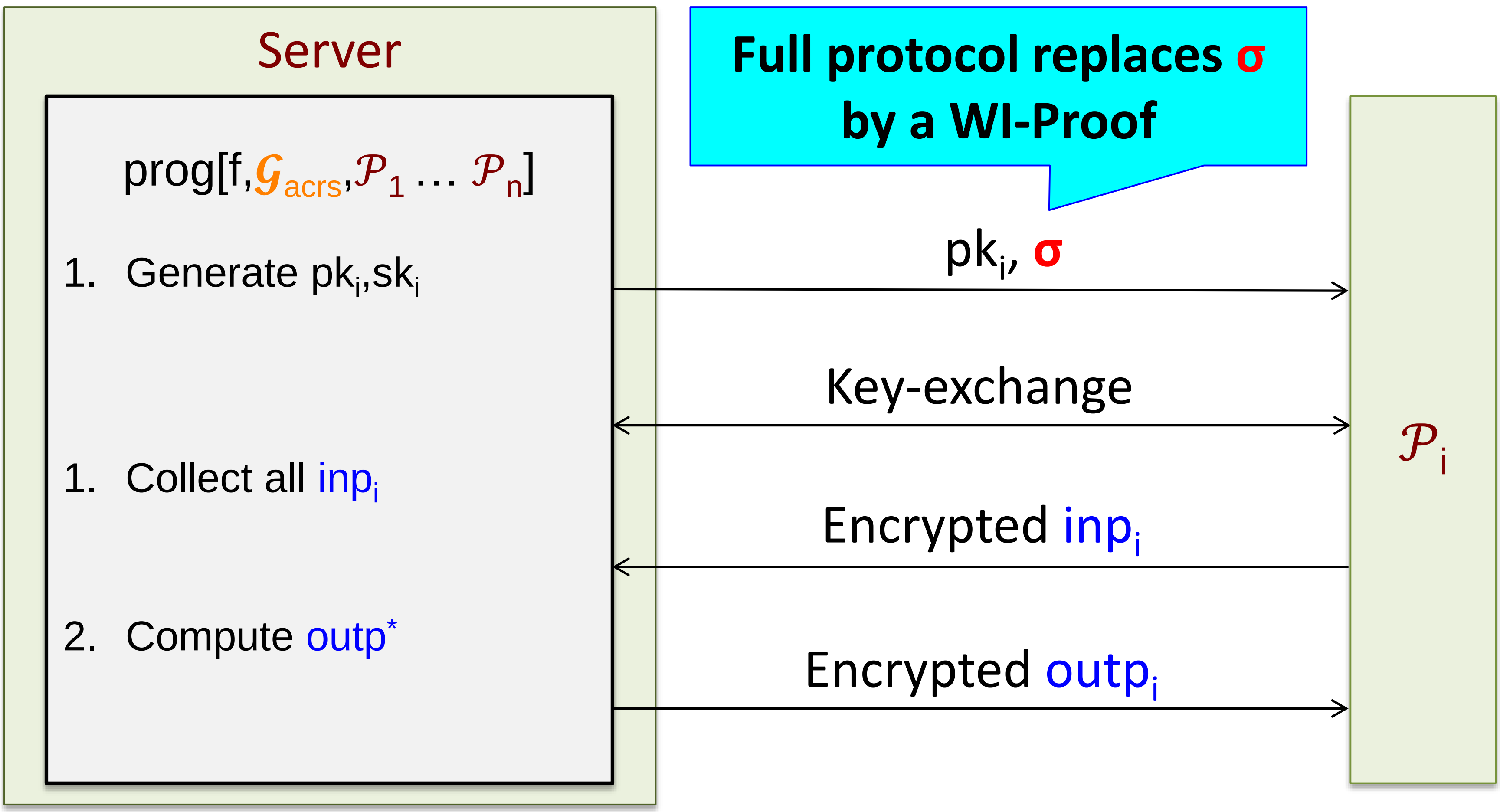

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3. Trapdoors

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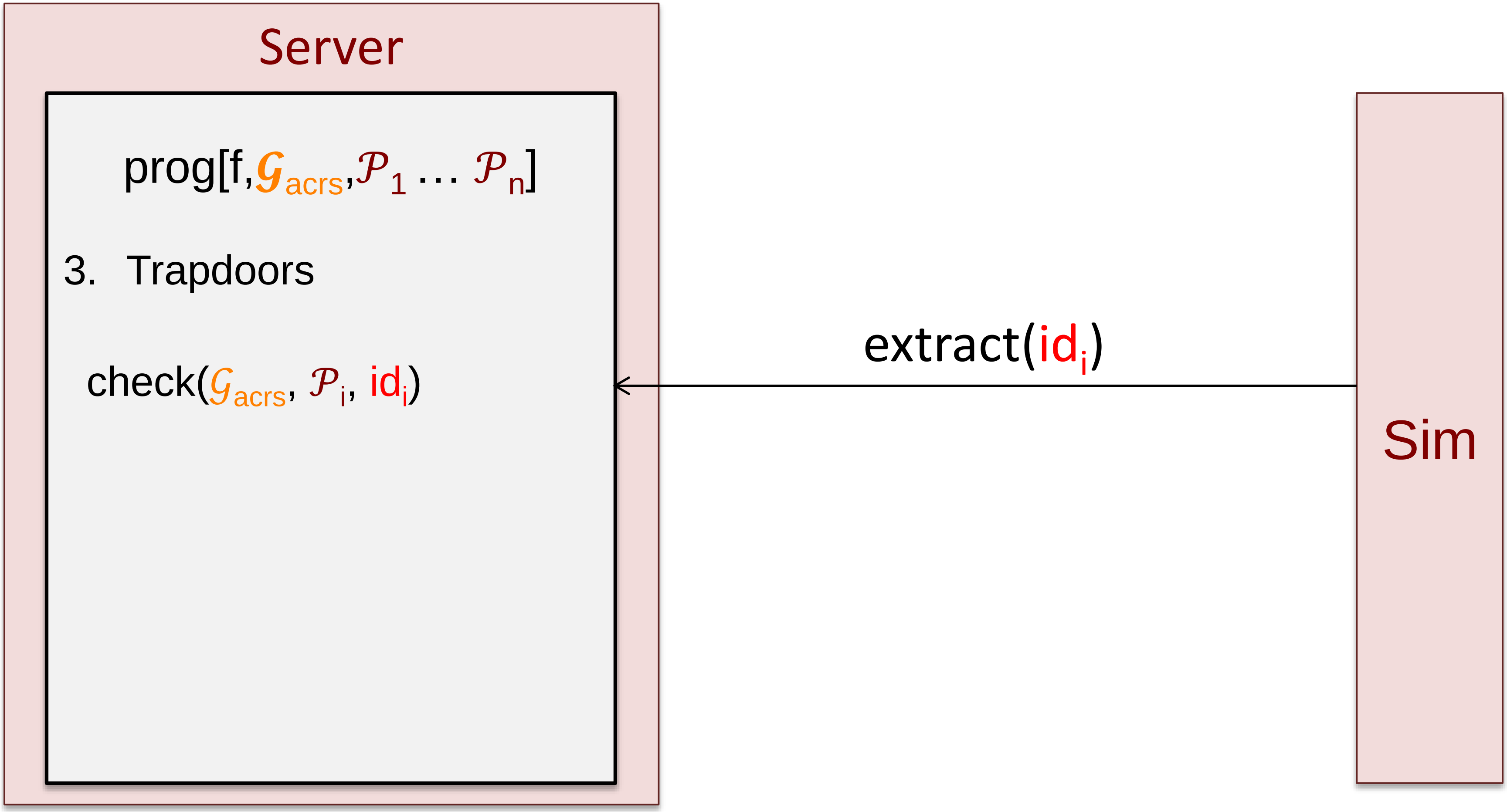

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check($\mathcal{G}_{acrs}$, $\mathcal{P}_i$, id_i)

Sim can recover inp$_i$

extract(id_i)

sk_i

Sim

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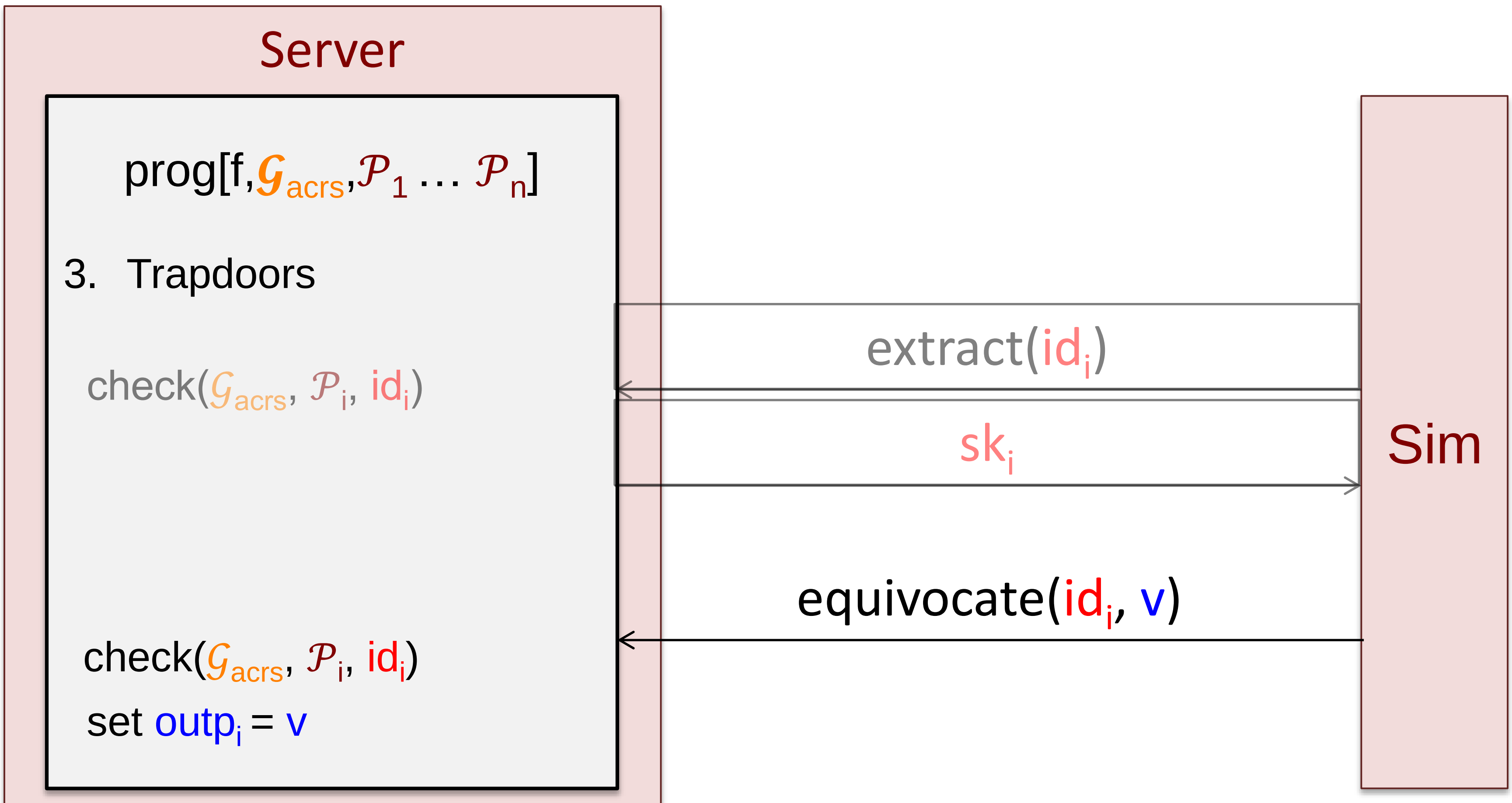

Fair 2PC

- Fairness impossible for general functionalities in plain model [Cleve86]

Fair 2PC

Can trusted hardware help with fairness?

- Fairness impossible for general functionalities in plain model [Cleve86]

Fair 2PC

UC-Secure Fair 2PC

Enhanced model: Clock-aware secure processor

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- Fair coin-tossing possible if one party has clock-aware secure processors (+ ACRS)

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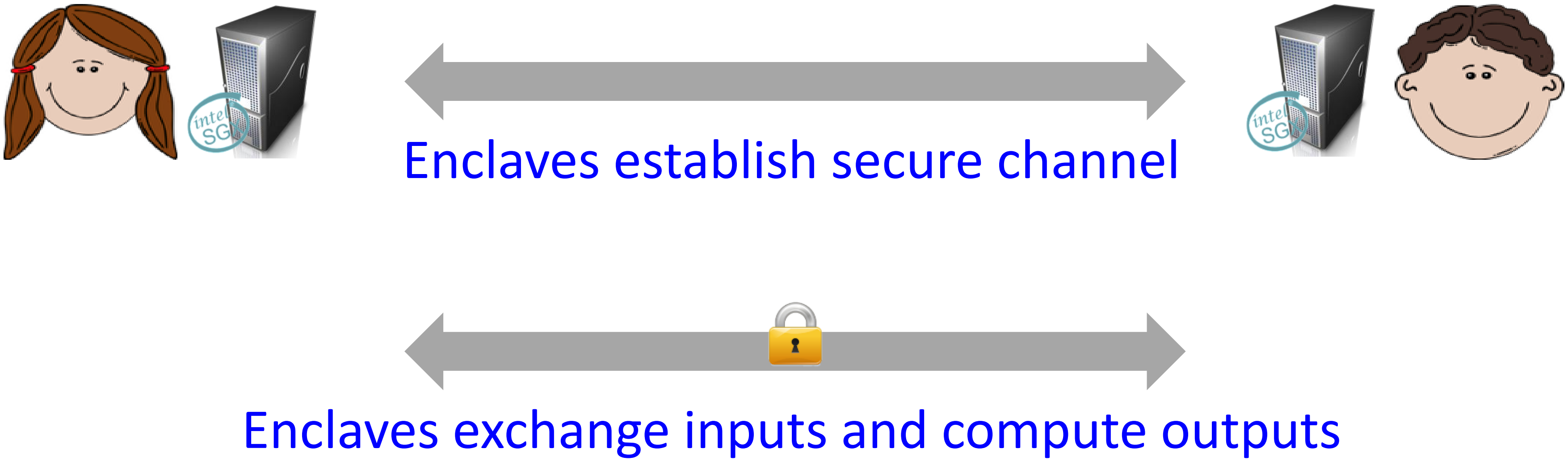
Enclaves establish secure channel


Enclaves establish secure channel
Enclaves exchange inputs and compute outputs
intel SGX
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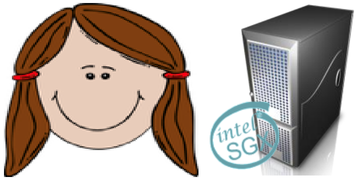

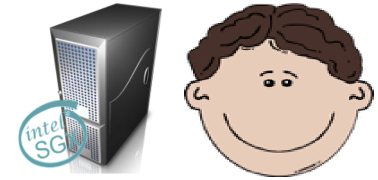

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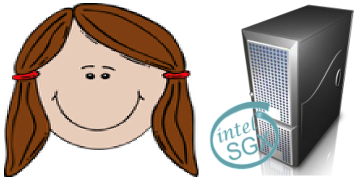
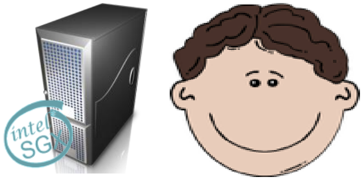
Enclaves exchange inputs and compute outputs

“Will release to Alice in 2^{λ} time”

“Will release to Bob in 2^{λ} time”





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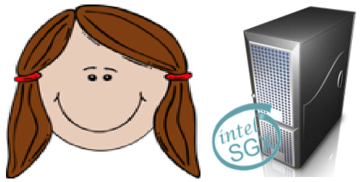

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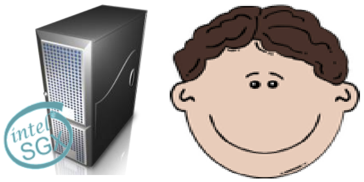

If Alice learns result at time $t < 2^{\lambda}$,

Bob will learn it at the latest by time $2t$

+ no "wasted" computation!

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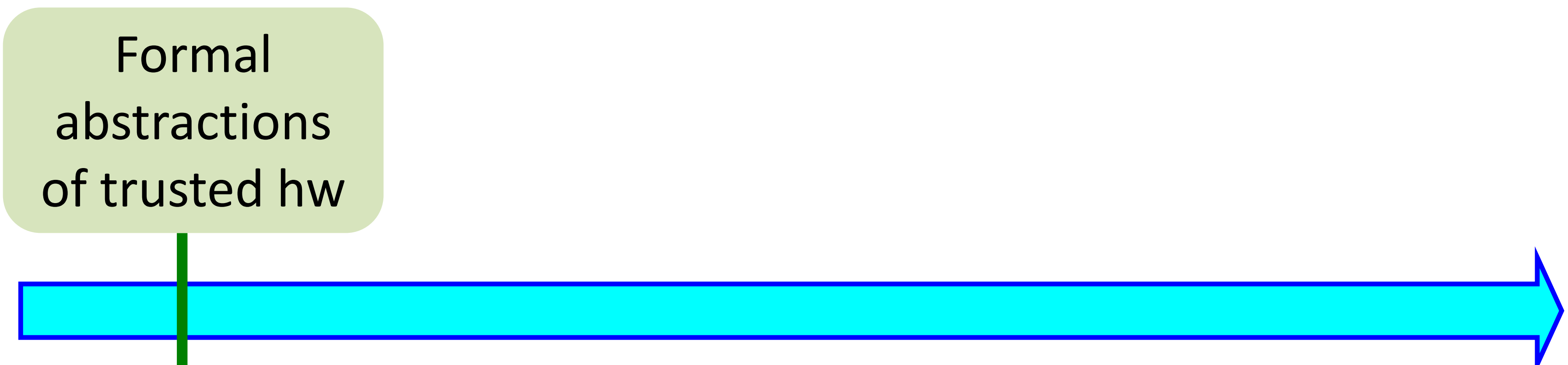
…

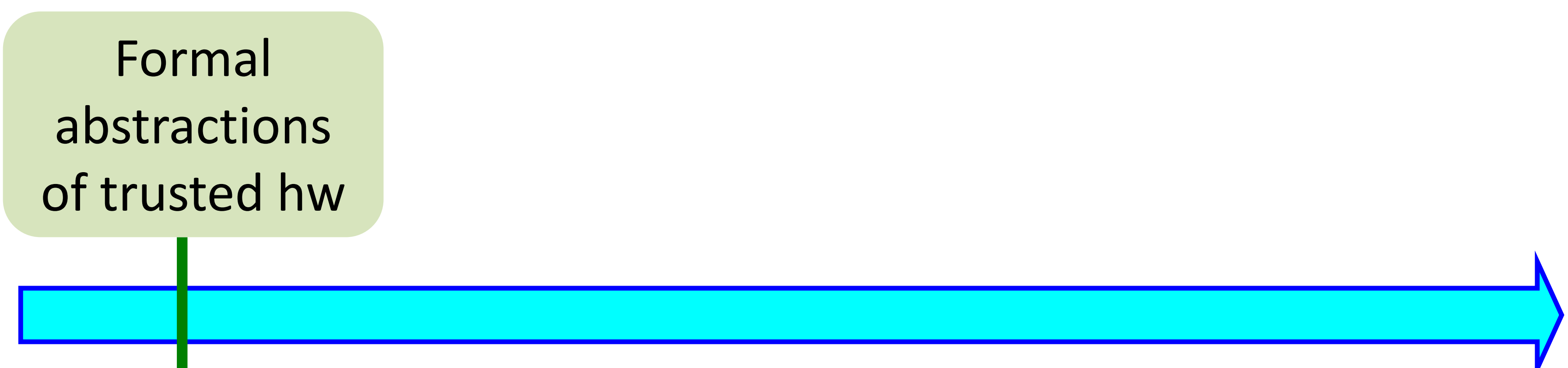
What next?



What next?

Attested execution is a powerful assumption

$\Longrightarrow$ Stateful Obfuscation, Efficient MPC, Fair 2PC



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$\Longrightarrow$ Non-deniability, Extra setup assumptions

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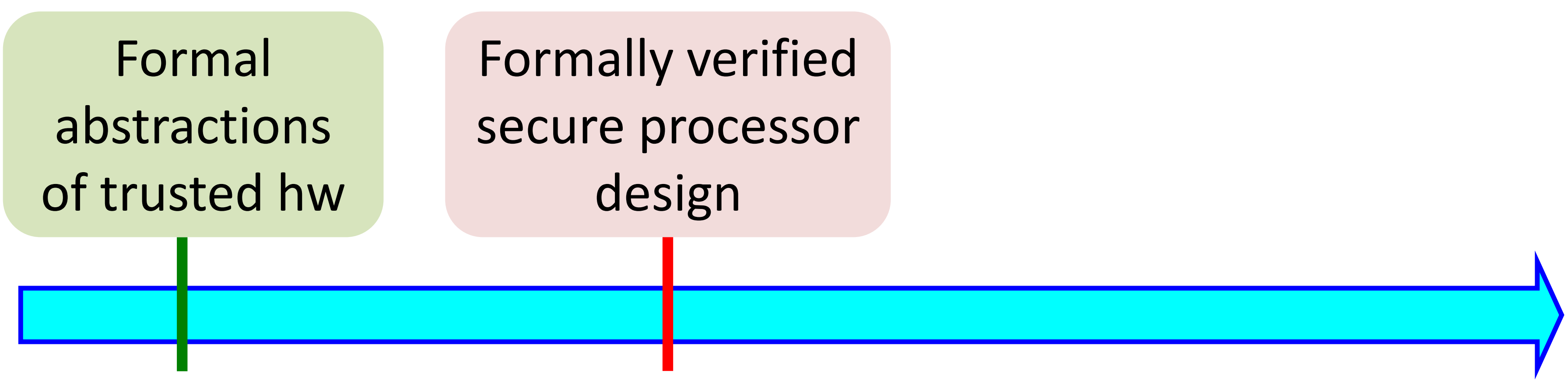

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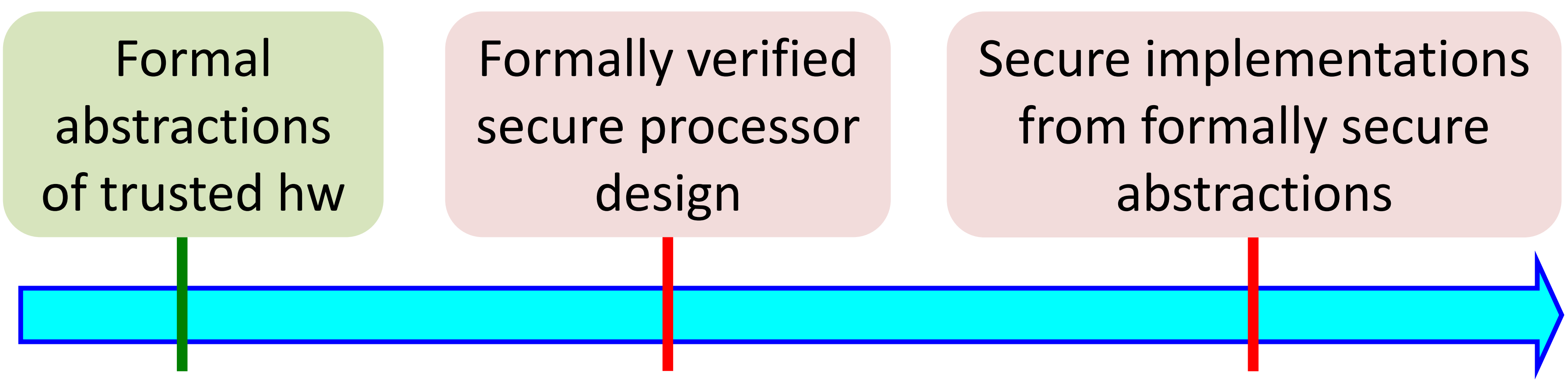
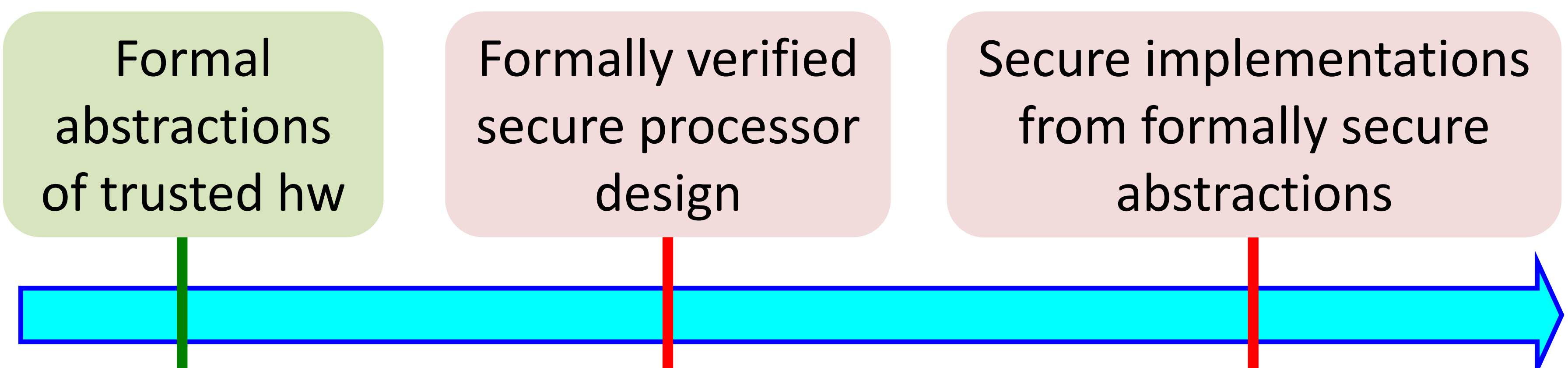


Thank You


Formal abstractions of trusted hw
Formally verified secure processor design
Secure implementations from formally secure abstractions